MODEL 800
TECHNICAL MANUAL

TECHNICAL
DESCRIPTION

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FUNCTION

The Robot Model 800 is a complete communications terminal for transmission and reception of Baudot, ASCII and Morse codes. In addition, the Model 800 will transmit an alphanumeric display via Slow Scan Television.

The heart of the Model 800 is an 8085 microcomputer. This microcomputer consists of the 8085 microprocessor supported by 6144 bytes of read only memory (ROM), 2048 bytes of video display memory, 512 bytes of random access memory (RAM), 7 parallel input/output ports (I/O), 1 serial I/O port and 2 14-bit timers. In addition to the microcomputer, the Model 800 contains an RTTY FSK (frequency shift keyed) demodulator, a sine wave synthesizer and a video display generator. Other than the actual demodulation of the RTTY FSK and Morse signals and the generation of the 72 character by 24 line display, all functions are performed by software in the microcomputer.

Received RTTY and Morse signals are fed to the Model 800 demodulator where they are filtered, conditioned and made compatible with the components in the microcomputer. They are then input to the microcomputer where they are decoded and displayed. Characters to be transmitted are read from the keyboard by the microcomputer. They are then converted into their corresponding codes and transmitted. In the Morse mode, transmission takes the form of keying the CW circuits of the users transmitter. In the RTTY and SSTV modes the signals take the form of audio tones formed by the sine wave synthesizer for transmission thru the audio circuitry of a transmitter.

Characters, received and transmitted, as well as all status information is displayed by the 72 character by 24 line video display generator. Additionally, in the SSTV mode, it provides a graphic display of the slow scan image being transmitted. The video display generator provides a composite video output for use with a conventional closed circuit television (CCTV) monitor. Vertical sync pulses from the display generator also act as an interupt to the microcomputer for software synchronization purposes and for SSTV timing.

The following RTTY speeds and codes are supported by the Model 800 as listed in Table A-1. The WPM figure listed, is that which is referred to by the industry and in some instances may be inconsistent with the remaining data.

CODE TYPE	WPM	BAUD	UNIT LENGTH	UNITS	START PULSE	STOP PULSE	TOTAL LENGTH
Baudot	60	45.5	22.0ms	5	22.0ms	33.0ms	165.0ms
Baudot	66	50.0	20.0ms	5	20.0ms	30.0ms	150.0ms
Baudot	75	56.8	17.6ms	5	17.6ms	26.4ms	132.0ms
Baudot	100	74.1	13.5ms	5	13.5ms	20.3ms	101.3ms
Baudot	132	100.0	10.0ms	5	10.0ms	15.0ms	75.0ms
Ascii	100	110.0	9.1ms	8	9.1ms	18.2ms	100.1ms

Table A-1
RTTY CODE AND SPEED STANDARDS

Transmission and reception of RTTY signals in the Model 800 is via a series of keyed electronic pulses. These pulses take the form of a serial stream of binary digits called bits, each bit consisting of either a binary "1" or mark, or a binary "0" or space. Each character as it is transmitted is preceeded by a space pulse called a start bit. This start bit aids in the synchronization of the transmitter and receiver. The start bit is followed by either a 5 bit code in the case of Baudot or 8 bits in Ascii. Each code consists of a series of mark and space bits that uniquely define a character. The extra bits in the Ascii code allow for the lower case alphabet and some additional punctuation not available in the Baudot code. Following the 5 or 8 bit code is a mark pulse called the stop bit. The stop bit signifies the end of the character. Any gap between the end of one character and the start of the next is filled with a continuous stream of mark pulses.

For ease of transmission the mark and space pulses are converted to audio tones. The mark pulse keys one tone, and the space another. The mark and space tones can then be directly fed into the audio input of a transmitter for transmission and can be received from the audio output of the receiver. This greatly simplifies the installation of the Model 800 as it is equivalent to adding an additional microphone and speaker to your station.

The difference between the mark and space tones is referred to as the "shift." There are three such shifts commonly in use. These are 170, 450 and 850 Hz shift. 170 and 850 Hz shift are commonly used by amateur radio operators and the 425 Hz shift typically used by commercial stations. The Model 800 has a set of filters, called discriminators, for reception of both 170 and 850 Hz shift. The 425 Hz commercial shift can be received using the 850 Hz shift discriminator by a process known as "straddle tuning". The signal to be received is tuned such that it falls in between the 850 Hz mark and space frequencies and is straddling the midpoint of the 850 Hz shift. The Model 800 however, only transmits 170 Hz and 850 Hz shift signals.

The standard Model 800 uses the IARU standard for the frequency of the mark and space tones. This standard is called "low-tone". The Model 800H uses the common American VHF-FM RTTY tone standard referred to as "high-tone". Table A-2 lists the mark and space frequencies employed for both the "low-tone" and "high-tone" frequency standards.

Low-Tone Pairs:
170 Hz SHIFT - 1275 Hz MARK, 1445 Hz SPACE
850 Hz SHIFT - 1275 Hz MARK, 2125 Hz SPACE
High-Tone Pairs:
170 Hz SHIFT - 2125 Hz MARK, 2295 Hz SPACE
850 Hz SHIFT - 2125 Hz MARK, 2975 Hz SPACE

Table A-2
LOW-TONE AND HIGH-TONE FREQUENCY STANDARDS

The existence of the two frequency standards gives rise to an apparent compatibility problem. This problem exists on VHF-FM where the actual audio tone is transmitted and tuning will not change the pitch of the received tones. However, the incompatibility does not exist on the HF bands. Here the AFSK signal is transmitted via a single sideband transmitter with the carrier and opposite sideband suppressed. This results in an RF signal that shifts an amount equal to the AFSK shift used. On reception the single sideband receiver reinserts a carrier so as you tune across the RTTY signal you can change the pitch of the received audio tones to any frequency desired.

The low-tone standard came into existence due to the limited audio bandwith of single sideband equipment. In some equipment the bandpass has been limited to that which is just necessary for normal speech (approximately 300-2400 Hz). The low-tones fall nearly in the middle of this audio bandpass, whereas the high-tones are quite near the edge and are often attenuated if not eliminated entirely as in the case of the 850 Hz space tone (2975 Hz). Straddle tuning of the 425 Hz commercial RTTY can be difficult if not impossible in some instances with high-tones.

Reception of Morse code in the Model 800 is accomplished by using the RTTY 170 Hz shift mark filter in conjunction with some software processing. The software algorithm tracks the incoming code over the range of 4 to 99 words per minute (WPM). The received code speed is displayed in the status line and is computed according to formula A-1. The Morse transmit timing is also related to this formula.

$$\text{Speed (WPM)} = \frac{1200}{\text{Dot Time (ms)}} \qquad \text{(A-1)}$$

Slow scan television generation is a software function in the Model 800. The SSTV image is continuously displayed by the video display generator in real time allowing for easy composition. The only auxiliary hardware used in this mode is the sine wave synthesizer circuitry for frequency modulation. Actual slow scan transmission takes the form of an audio FM signal that deviates between 1500 Hz (black) and 2300 Hz (white). Slow scan synchronization pulses are at 1200 Hz. Standards for SSTV timing are slightly different for 50 Hz countries than those for 60 Hz. The Model 800 will support either one of these standards as specified at time of purchase. Table A-3 lists the SSTV timing for both 60 Hz and 50 Hz units.

	60 Hz	50 Hz
Line Time	66.6ms	60.0ms
Frame Time	8.5s	7.7s
Horz Sync Time	6.1ms	6.1ms
Vert Sync Time	66.6ms	60.0ms

Table A-3
60 Hz and 50 Hz SSTV Timing

BLOCK DIAGRAM

An overview of the internal operation of the Model 800 is shown in Figures B-1 and B-2. For clarity the block diagram is divided into two sections, Figure B-1, the digital section and Figure B-2, the analog section. The digital section can be subdivided as the microcomputer and video display sections, the microcomputer being shown in the top half of Figure B-1 and the video display on the lower half.

DIGITAL SECTION (Figure B-1)

The heart of the microcomputer section is the central processing unit (CPU) as shown in Block 1. It executes the preprogrammed instructions contained in the read only memory (ROM) of Block 3. The preprogrammed instructions called software, perform the operational functions of the Model 800 such as the decoding of the Morse and RTTY characters after they are demodulated, transmitting characters to be sent, reading the keyboard for character entries, controlling the video display, etc.

Random access memory (RAM) is used for temporary storage and for the buffering of incoming and outgoing information. The RAM is found in Blocks 5 and 6 as well as input/output channels (I/O) and the two 14-bit programmable interval timers.

The input/output channels or ports, are used to interface the microcomputer to other hardware modules in the Model 800. The input/output function in Block 5 is dedicated to interfacing the microcomputer to the keyboard. This allows the microcomputer to scan the keys for entry and subsequent decoding of keyboard entries as shown in Block 5a. The input/output section of Block 6 is used to interface the analog demodulator, tuning indicator, sidetone oscillator, sine wave synthesizer and various solid state switches.

The two 14-bit timers of Blocks 5 and 6 provide almost all of the timing functions within the microcomputer. The timer in Block 5 is typically used as the USART (universal syncronous/asyncronous receiver/transmitter) clock for the reception of demodulated RTTY signals or as a programmable frequency source for the sine wave synthesizer. The timer in Block 6 is tied to an Interrupt line on the CPUand allows for the accurate timing and control of some of the more dynamic software rountines, such as Morse receive and transmit speed control, RTTY transmit baud rate generation and SSTV pixel and sync pulse timing.

All information between devices in the microcomputer is transferred over information buses. There are three such buses in the Model 800 microcomputer, an address bus for the selection of devices, a data bus for the transfer of information between devices and a control bus for the orderly transfer of information and issuance of addresses on their respective buses.

The video display memory, shown as Block 14, is a 2048 byte random access memory. The entire 2048 bytes can be accessed by the mirrocomputer through the data bus controller and the address multiplexer, Blocks 8 and 13 respectively. The bus controller assures that the microcomputer does not access the memory at the same time as the video display generator thereby eliminating disturbances on the video display. The conflict is avoided by only allowing the microcomputer to access the memory during video display sync times. The address multiplexer switches between the microcomputer address bus and the video display addressing circuits so that only one set of addresses are present at any one time to the video display memory. Again the addresses are only switched at sync times to avoid display interference.

The display size of 24 lines of 72 characters yields a total display of 1728 characters. Video display memory is arranged such that the first 1728 bytes of the total 2048 are those that store the characters to be displayed. These characters are stored in ASCII code (American Standard Code for Information Interchange) with an added bit, the most significant bit, to indicate the video polarity of the displayed character. Characters can be displayed as a matrix of white dots on a black background or as black dots on a white background as dictated by the video polarity bit. The remaining 320 bytes at the end of the video display memory are never displayed and therefore are available for temporary storage and information buffering.

The video display generation is controlled by the horizontal and vertical timing generators shown as Blocks 10 and 11 respectively. Both generators are directly referenced to the system clock, a crystal controlled frequency source, to assure display stability. The timing generators provide horizontal and vertical synchronization and blanking signals as well as addresses for accessing the video display memory.

The horizontal and vertical addresses are routed to the linear address generator where they are processed for proper control of the display memory. The linear address generator, Block 12, must address the display memory consistent with a horizontal raster scan format of character display. This format is illustrated in figure B-3. Each scan line forms one line of a character row, each character row containing 72 characters. A total of 9 scan lines are required to complete one row of characters. The linear address generator must therefore sequentially generate the address of each of the 72 characters in the row as the raster is scanned from left to right. Upon completion of the scan line the linear address generator must repeat this sequence, again starting with the address of the first character in the

row. The sequence is repeated a total of 9 times, completing the character row. Instead of starting with the address of the first character of the completed row, the address generator will continue on to the address of the first character of the next character row. This procedure is carried out for all 24 character rows of the display for each frame of the video display. A microcomputer loaded base register is examined at the beginning of the video frame and is used as the starting address of the first character row displayed. This allows for easy hardware scrolling of the display information.

As the display memory is being addressed its data is presented to the character generator, as illustrated in Block 15. The character generator is a 2048 byte read only memory programmed with the dot patterns representing each character. This dot pattern takes the form of a 7 by 9 dot matrix as shown in Figure B-3. The actual form of storage in the ROM allows one byte, or 8 bits, for every line of dots in the character. Since only 7 bits are required to store one line, the 8th bit is discarded. Each character is comprised of 9 lines of dots and therefore requires a 9 byte block of storage in the ROM.

The character data from the display memory acts as an address to the ROM, to select the actual 9 byte block of dots representing the character to be displayed. Signals from the vertical timing generator also act as addresses to select the proper line of dots, or byte, in the 9 byte block to be displayed. The selected line of dots appears at the output of the character generator ROM and is then loaded into a shift register, Block 16. The shift register, loaded with the 7 dots, shifts them out serially, a dot at a time as video information. On completion, the shift register once again is loaded with a line of dots representing one line of the next character to be displayed. This sequence is repeated for every line of every character in the display.

The resulting video information output by the shift register is combined with horizontal and vertical sync and blanking signals in the video combiner, as shown in block 17. The composite video output of the combiner is an EIA RS-270 compatible signal supplying 1.4 V p-p video into a 75 ohm load. Figure C-5 illustrates the characteristics of the video output. Horizontal and vertical timing specifications for 60 Hz and 50 Hz units are found in Table B-1.

	60Hz	50 Hz
Line Time	63.86us	63.86us
Line Freq.	15660Hz	15660Hz
Frame Time	16.67ms	19.99ms
Frame Freq.	60.00Hz	50.03Hz
Lines/Frame	261	313
Horz Sync	5.00us	5.00us
Horz Blanking	18.78us	18.78us
Vert Sync	574.7us	574.7us
Vert Blanking	2.87ms	6.19ms

Table B-1
60 Hz and 50 Hz Video Timing

ANALOG SECTION (Figure B-2)

RTTY and Morse audio signals enter the Model 800 through the input level control. The input level control allows continuous attenuation of the input audio to provide for limiterless reception in the RTTY modes and to control threshold detection of the Morse signal. Following the input level control, the signal enters into a high-pass filter, as shown in Block 1. The high-pass filter suppresses lower frequency signals that may interfere with the signal of interest by capturing the limiter.

After passing through the high-pass filter the audio signal may take one or two paths. In the 170 Hz shift mode the signal deviates such a small percentage of the typical receiver's bandwidth that additional filtering above the frequency of interest is also helpful, therefore a low-pass filter is also provided in this mode, as shown in Block 2. This has the effect of a bandpass filter centered around the 170 Hz shift signal and in effect eliminates troublesome signals that may have been passed by the receiver's broad bandwidth. However, the 850 Hz space signal is so close to the upper frequency limit of the receiver bandwidth that further filtering would accomplish little. Therefore, in the 850 Hz mode, the signal is routed directly to the limiter stage, Block 3.

The limiter is a high gain amplifier that increases the input signal to a known level in preparation for demodulation. The limited signal is passed on to the mark and space discriminators, as illustrated in Blocks 4a through 4d. The discriminators separate the mark and space signals by passing the tone of interest and suppressing the other. The output of each discriminator is fed to the tuning indicator, as shown in Block 5. The tuning indicator is controlled by the microcomputer and processes the mark and space signals for display as the on screen tuning bar. The output of each discriminator also feeds a full wave rectifier to detect the mark and space pulses. The full wave rectifiers are shown in Blocks 6a and 6b. The mark is detected as a positive voltage and the space as a negative voltage. The mark and space voltages are then combined and filtered in the low-pass filter shown in Block 7. The low-pass filter removes the high frequency carrier component of the mark and space signals and yields a bipolar base-band signal containing only mark and space information.

The base-band mark and space information is corrected such that the positive and negative excursions are of equal amplitude. This function is accomplished by the automatic threshold computer shown in Block 8. The action of the automatic threshold computer helps correct amplitude distortion due to selective fading. The corrected base-band information is presented to the slicer, Block 9. The slicer, an open loop amplifier, squares up the distorted but amplitude corrected pulses and conditions them for TTL (Transistor Transistor Logic) compatibility. Once TTL compatible, the signal is input to the serial channel of the microcomputer for decoding and display.

The sidetone oscillator, shown in Block 10, is used for several purposes. In the Morse receive mode it can be used as a tuning aid by zero-beating the incoming signal with the sidetone output. It also acts as a morse code regenerator and indicates exactly what the microcomputer is receiving at any given moment. In the Morse transmit mode it acts as a sidetone oscillator and indicates the code being transmitted. In the RTTY mode it acts as an end of line indicator and beeps upon entry of the 64th character in a line. It also is used to indicate a buffer full condition when typing ahead in the transmit buffer.

The sine wave synthesizer, shown in Block 11, is used in the generation of the audio tones for the audio frequency shift keying of the RTTY signal. It is also used for the generation of the audio FM slow scan television signal. The sine wave synthesizer provides a clean, low distortion audio output for subsequent transmission through the audio circuitry of the host transmitter.

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CIRCUIT DESCRIPTION

DIGITAL SECTION

BLOCK 1. CENTRAL PROCESSING UNIT

The central processing unit (CPU) is the 8085A microprocessor. The 8085A (U1) controls all functions within the Model 800. The 8085A transfers data on an 8-bit bi-directional tri-state bus (AD0-AD7). This bus is time multiplexed to also provide the least significant 8 bits of address. The most significant 8 address bits are provided directly and are labeled as A8-A15. The 16 bits of address provided allows the addressing of up to 64K bytes of memory although only a fraction of this is actually used in the Model 800.

The 8085A CPU also generates a set of controls that are used to select various peripheral devices and to perform read and write to these devices and memory. A maximum of 255 input/output (I/O) devices can be addressed using AD0-AD7, the IO/M line determining whether the address is for I/O or memory.

Five interrupts are available on the 8085A, RST 7.5, RST 6.5, RST 5.5, INT and TRAP. The Model 800 only exercises the first three. Both the INT and TRAP interrupts are tied to ground and therefore disabled. RST 7.5 is tied to the timer output of U2 and provides a programmable time interrupt for the CPU. RST 6.5 is tied to the RxRDY output of U7, the 8251A USART (Universal Syncronous Asyncronous Receiver/Transmitter), and interrupts the CPU when ever the 8251A has a received character to transfer. RST 5.5 is tied to VERT LOAD (U44-4) and interrupts the CPU at the start of vertical blanking in the video display generator.

The CPU READY/WAIT line is attached to U35-6 and allows the reading and writing of display memory information without disturbing the display. This is accomplished by forcing the CPU to wait until horizontal sync before accessing the display memory.

The combination of R4 and C2 provide a power on reset of the CPU and insure an orderly start-up.

A 5.6MHz clock source is provided at U38-12 and serves as the processor clock for the 8085A.

All 8085A control signals and busses are brought out to connectors at the main PC board edge for possible future expansion.

BLOCK 2. ADDRESS LATCH

U4 performs the demultiplexing of the lower 8 bits of address multiplexed with data on the AD0-AD7 lines of the 8085A. On the trailing of ALE (Address Latch Enable) the lower 8 bits of address are stable on the data bus. U4 latches this address data on the trailing edge of ALE and provides address bits A0-A7. These bits in conjunction with A8-A15 on the 8085A provide a full 16-bit address bus. The 8085A signal HLDA (Hold Acknowledge) is connected to U4-1, tri-state enable. This allows the 8085A to tri-state U4 along with A8-A15 and AD0-AD7 during processor HOLD states.

BLOCK 3. ADDRESS DECODER

Device selection is accomplished by decoding the address of the device as it is placed on the address bus. U19, a 1-of-8 decoder, accomplishes this task by decoding 8 2048-byte blocks of address space. Outputs CS0-CS7 indicate the block being addressed at any given time. U42 combines CS0 and CS1 to form a chip select for 4096-byte memorys.

BLOCK 4. ROM—READ ONLY MEMORY

The Model 800 presently incorporates 6K (6144) bytes of program memory stored in ROM. The 6K memory is composed of U5 a 4K ROM and U6 a 2K ROM. U5 resides in the first two 2048 blocks of memory and therefore is selected by the combination of CS0 and CS1 formed by U42. U6 is selected directly by CS2 and resides in the third block of memory. The 8085A RD (Read) control line assures that U5 and U6 only output information on the data bus at read times.

BLOCK 5. 8155—RAM, I/O AND TIMER (#1)

U3, an 8155, is a combination peripheral chip that performs several functions. Included is a 256-byte random access memory (RAM), two 8-bit input/output (I/O) ports, one 6-bit I/O port and a 14-bit programmable interval timer. The 256-byte RAM is used for temporary storage by various software routines and for keyboard character buffering.

The first 8-bit I/O port, Port A, is an output port and is used to scan one side of the key matrix of the keyboard. The second 8-bit I/O port, Port B, is an input port and is connected to the other side of the matrix. By scanning Port A, while reading Port B, a depressed switch can be isolated and decoded. The layout of the key matrix is illustrated in Figure C-1.

The 6-bit I/O port, Port C, is an input port and is used to read the special keys not included in the key matrix. PC0 (K0) is connected to the two shift keys. PC1 (K1) is connected to the control (CTRL) key. PC2 (K2) is connected to the escape (ESC) key. PC3 (K3) is connected to the repeat key. PC4 (K4) is connected to the upper case CAPS LOCK key. PC5 is not used and is spare.

The 14-bit programmable interval timer is used by the software for external timing purposes. The timer clock input is tied to the 8085A clock output CLK which has a period of 358ns. The output of the timer, DATA CLK, is connected to the clock input of the 8251A USART (U7) and the clock input of the sine wave synthesizer (U48). Thus it can become either a programmable baud rate generator for USART operations or a programmable frequency generator for frequency shift keying or frequency modulation with the sine wave synthesizer.

CS6 enables this device for transfer of information on the 8085A data bus.

BLOCK 6. 8155—RAM, I/O AND TIMER (#2)

U2, an 8155, is a combination peripheral chip that performs several functions. Included is a 256-byte random access memory (RAM), two 8-bit input/output (I/O) ports, one 6-bit I/O port and a 14-bit programmable interval timer. The 256-byte RAM is used for temporary storage by various software routines and for keyboard character buffering.

The first 8-bit I/O port, Port A, is an input port. PA0 is tied to the tuning indicator end of conversion, or EOC, pin. This signal indicates that analog-to-digital (A/D) conversion is complete. PA1 is connected to RxD (Received Data) of U64 in the demodulator and allows the computer to examine incoming demodulated data. PA2 looks at the ZERO output of the sine wave synthesizer allowing the microcomputer to change the sine wave frequency at zero-crossing times. PA3 through PA6 are not used presently and are spare. PA7 receives the keypressed (KP) strobe from the keyboard interface, indicating that a key has been depressed and should be read.

The second 8-bit I/O port, Port B, is an output port. PB0 is tied to RCV/XMT of Q5 and controls the receive/transmit switching. PB1 is connected to 170/850 of U51 and U58 and controls the 170 Hz and 850 Hz filter selection. PB2 is connected to REV/NOR of U64 and controls received mark and space polarity. PB3 is tied to RESET of U48 and disabled and resets the sine wave synthesizer. PB4 through PB7 are not used and are spare.

The 6-bit I/O port, Port C, is an output port. PC0-PC2 are labeled B1, B2 and B3 and are the three data lines that connect to the tuning indicator D/A (Digital Analog) converter, U47. PC3 labeled BELL is connected to the sidetone oscillator and controls the bell function and the Morse code sidetone. PC5 is not used and is spare.

The 14-bit programmable interval timer is used by the software for internal timing purposes. The timer clock is the first term of the character counter, H0 of U14. This signal provides a 1.2521us clock. The output of the timer is connected to RST 7.5 of the 8085A and therefore provides a programmed interrupt.

CS7 enables this device for transfer of information on the 8085A data bus.

BLOCK 7. USART—UNIVERSAL SYNCHRONOUS/ASYNCRONOUS RECEIVER/TRANSMITTER

U7 is an 8251A USART and provides a serial input/output channel for the 8085A. In the receive mode information from the demodulator through U64 is loaded serially into the 8251A and transferred over the data bus to the 8085A. In the transmit mode, information from the 8085A is sent serially through the USART to the TTY LOOP keyer (Q5) for hard copy output. The U3 timer output provides a receive and transmit clock for the USART.

CS3 enables this device for transfer of information on the 8085A data bus.

BLOCK 8. BUS CONTROLLER

Bi-directional bus drivers U20 and U21 allow for the sharing of the video display memory data bus between the 8085A and the video display generator. At horizontal blanking times U36 and U37 allow the 8085A data bus to extend to the video display memory through the bi-directional bus drivers for display read and write. By limiting access to blanking time, display disturbance is eliminated.

U35 forces the 8085A to wait until sync time before executing the actual read or write operation via the 8085A READY/WAIT line.

CS4 enables this device for transfer of information on the 8085A data bus.

BLOCK 9. SYSTEM CLOCK

The system clock is a 11.181240 MHz crystal controlled oscillator that is used to control all timing functions in the Model 800. U45 is configured as a non-inverting amplifier with Y1, a series resonant crystal providing the feedback path for oscillation. U38 buffers the system clock which is used directly by the video display circuitry as a character dot clock. This signal is divided in half by U39 to 5.590620 MHz for use as the 8085A processor clock (PCLK).

BLOCK 10. HORIZONTAL TIMING

The 11.181240 MHz dot clock is fed to U13, a divide-by-7 counter. U13 allows 7 dot times to occur for the transmission of serial video out of video shift register U23. Upon completion of 7 dot times U13 reloads and the load pulse forms the character clock (CC).

Figure C-2 illustrates the horizontal timing relationships.

U14 and U15 are initially loaded to 226 at the start of horizontal blanking by U33. Horizontal blanking is generated by term H7. The counter then counts up a character at a time by clock CC. U34-6 decodes the start of horizontal sync at state 236 and sets flip-flop U37. U34-12 decodes the end of sync at state 244 and resets U37. At state 256 the counter overflows to state 0, horizontal blanking ends and horizontal live time begins. A line of 72 characters is displayed during states 0-71. U33 decodes state 71 and causes the loading of the counter and the beginning of blanking at the next state.

BLOCK 11. VERTICAL TIMING

—60 Hz UNITS

Horizontal blanking, term H7, is fed as a clock to the character row line counter U16. U16 is a divide-by-9 counter and generates the 9 line addresses required to access the 9 byte character dot pattern in the character

generator ROM, U31 decodes the first line, LINE 0, of each character row. At the end of 9 lines U16 reloads and generates a character row clock for the character row counter, U17 and U18.

The character row counter is initially loaded to a count of 251 at the start of vertical blanking by U44. Vertical blanking is generated by term V7. The counter then counts up a character row at a time. U34 decodes the start of vertical sync at line 4 of state 252 and sets flip-flop U40. U40-11 decodes the end of sync at line 4 of state 253 and resets U40. At state 256 the counter overflows to state 0, vertical blanking ends, and vertical live time begins. 24 rows of characters are displayed during states 0-23. U44 decodes state 23 and causes the loading of the counter and the beginning of blanking at the next state.

Figure C-3 illustrates 60 Hz vertical timing relationships.

—50 Hz UNITS

Horizontal blanking, term H7, is fed as a clock to the character row line counter U16. U16 is a divide-by-9 counter and generates the 9 line addresses required to access the 9 byte character dot pattern in the character generator ROM. U31 decodes the first line, LINE 0, of each character row. At the end of 9 lines U16 reloads and generates a character row clock for the character row counter, U17 and U18.

The character row counter is initially loaded to a count of 245 at the start of vertical blanking by U44. Vertical blanking is generated by term V7. The counter then counts up a character row at a time. U34 decodes the start of vertical sync at state 250 and sets flip-flop U40. U40-11 decodes the end of sync at state 251 and resets U40. At state 256 the counter overflows to state 0, vertical blanking ends, and vertical live time begins. 24 rows of characters are displayed during states 0-23. U44 decodes state 23 and causes the loading of the counter and the beginning of blanking at the next state.

Figure C-4 illustrates 50 Hz vertical timing relationships.

BLOCK 12. LINEAR ADDRESS GENERATOR

The linear address generator consists of three basic sections, the base register, the row address register and the character counter. U8 is an 8-bit latch, selected by CS5. The 8085A loads the address of the character row to be displayed as the bottom row of the display into U8. The linear address generator uses this as a base for all video display addressing thus providing an efficient form of display scrolling.

U10 is the row address register and contains the address of the first character of the present character row being displayed. This address will be loaded into the character counter at the beginning of each of the 9 lines of a character row.

U9 and U11 compose the character counter. At the beginning of a scan line the counter is loaded with the starting address of the first character in the present character row. It then counts up 72 characters from that point 8 characters at a time with the aid of U42 and U32 as a clock. Only address bits of a higher order than the first 3 need be linearized as the first 3 bits (H0, H1 and H2) follow a linear sequence from line to line. The first three bits will always start at 000 at the beginning of a line and therefore can be used directly for memory addressing. The other bits C0-C7 must be stored as they have a unique value for the start of each character row. At the completion of the 72 character line the starting address stored in U10 is loaded into the counter for the next scan line. This is repeated for the 9 lines comprising a character row. At the end of the 9th scan line of the character row, the address is allowed to increment to the address of the first character of the next row under the control of U40. The new address is stored in U10 replacing the starting address of the last row. The storage operation is executed by the clocking action of U37. This sequence is repeated for all 24 character rows.

U12 detects an end of memory situation at address 1728 (24 X 72) and resets the character counter.

At vertical blanking U10 is disabled and U8 the base address register, is again loaded starting the address sequence.

BLOCK 13. ADDRESS MULTIPLEXER

U24, U25 and U26 form the video display memory address multiplexer. At horizontal blanking times control signal HB switches the 8085A address bus on to the video display memory address inputs. This allows the 8085A to address the memory for read write purposes during blanking. At all other times the multiplexer switches the linear address generator and H0, H1 and H2 on to the video display memory address bus for video display generation.

BLOCK 14. VIDEO DISPLAY MEMORY

U27 through U30 comprise the video display memory. The memory chips are 1K-by-4 bit static random access memories and are configured as a 2048-by-8 bit memory.

BLOCK 15. CHARACTER GENERATOR

U22 is a 2K-by-8 bit read only memory and is programmed as a character generator for addressing by the video display circuitry. U22 contains the dot matrix patterns for all alphanumeric and graphic characters displayed by the Model 800.

Lines D0-D6 provided by the video display memory data outputs, select the character to be displayed. Lines R0-R3 are generated by the vertical timing generator and select the proper line of dots within the character to be output by the generator.

BLOCK 16. VIDEO OUTPUT SHIFT REGISTER

U23 loads the parallel dot information from U22 the character generator and shifts it out serially a dot at a

time. Every seventh character the character clock CC loads the shift register with new information from the character generator. The dot clock shifts a new dot out of the shift register every 89ns. The output of the shift register is exclusive—or'd with D7, the video polarity bit, from the video display memory and provides normal/reverse video switching. The output of the exclusive or gate U32 is re-clocked for final video output by U39 and the 11.181240 MHz dot clock.

Horizontal and vertical blanking is combined and generated by clearing U23 during blanking times. U36 combines the two blanking signals while U39 synchronizes them with the operations of U23.

BLOCK 17. VIDEO COMBINER

Video and sync signals are combined for final video output by the video combiner U41. U41 is an open collector gate and allows the video and sync signals to be combined by the resistor network containing R5, R6 and R8. The composite video signal is buffered by emitter follower Q1. The network R7, C3 and C4 provide power supply isolation of the output stage. Video output is taken across emitter resistor R9 through R24 and provides a 1.4 V P-P output into 75 ohms. The composite video output is illustrated in figure B-4.

ANALOG SECTION

BLOCK 1. HIGH-PASS FILTER

U50 is configured as a fourth order 1dB Chebyshev high-pass filter. The 3dB point is approximately 1200 Hz for low-tone Model 800's and 2000 Hz for high-tone units. The filter has a gain of 5. Diodes CR5 and CR6 are for protection from excessive input signal amplitude.

BLOCK 2. LOW-PASS FILTER

U52 is configured as a fourth order 1dB Chebyshev low-pass filter. The 3db point is approximately 1540 Hz for low-tone Model 800's and 2430 Hz for high-tone units. The filter has a gain of 5.

BLOCK 3. LIMITER

U54 and U53 form a limiting amplifier with a gain of 10. The actual signal limiting is accomplished by diodes CR7 and CR8. Limiting occurs at 1.4 V p-p. The overall gain of the input stages is 250 at 170 Hz shift and provides limiting at a 5mV signal level. At 850 Hz low-pass filter U52 is switched out by analog switch U51 and the input gain correspondingly drops by a factor of 5 to a gain of 50. This still provides adequate limiting of 850 Hz signals down to a 25mV input signal level.

BLOCK 4. DISCRIMINATORS

U59 through U62 are the 170 Hz and 850 Hz mark and space discriminators. Each discriminator filter is a second order positive feedback bandpass filter. U59 is the 850 Hz mark filter, U60 the 170 Hz mark, U61 the 850 Hz space and U62 the 170 Hz space. 170 Hz mark and space filters have a bandwidth of approximately 96 Hz while the 850 Hz filters have a bandwidth of about 212 Hz. The low-tone filters have a gain of 6, high-tone units a gain of 18.

R69 and R96 are the discriminator balance controls and allow for the accurate compensation for possible differences in gain between the mark and space filters.

BLOCK 5. TUNING INDICATOR

The tuning indicator is comprised of two major components, a peak detector and an analog-to-digital (A/D) converter. The peak detector samples the outputs of the mark and space discriminators while the A/D measures the resultant peak voltage. The computer supervises the A/D conversion by outputing a 3-bit binary value (B0-B2) to the digital-to-analog (D/A) network comprised of resistors R37-R40. This analog voltage is compared with the mark and space voltage from the peak detector with comparator U47. When the microcomputer outputs the proper 3-bit value equal to the peak detected voltage the comparator trips indicating the proper value has been found. The microcomputer uses this value for display in the tuning bar.

BLOCK 6. FULL WAVE RECTIFIERS

The two sections of U57 form full wave rectifiers for the detection of the mark and space information. The two sections of analog switch U58 switch between the 170 Hz and 850 Hz filter outputs for input to the full wave rectifiers.

BLOCK 7. LOW-PASS FILTER

U56 is configured as a low-pass filter for the recovery of the baseband mark and space information. This filter is a fourth order Butterworth filter with a cutoff frequency of 70 Hz and a gain of 2.6.

BLOCK 8. AUTOMATIC THRESHOLD COMPUTER

The output of low-pass filter U56 is input to the automatic threshold computer comprised of capacitors C33 and C34, diodes CR11-CR14 and resistors R114 and R115. This network peak detects the mark and space pulses and biases the signal such that the positive mark and negative space pulses are symetrical about zero volts.

BLOCK 9. SLICER

U54 is an open loop amplifier, called a slicer. The slicer converts the incoming bi-polar mark and space signal to a 24V p-p square wave. This square wave is then made TTL (Transistor Transistor Logic) compatible by the network containing R119, CR15 and CR16. The TTL compatible signal is input to exclusive or gate U64 and subsequently input to the microcomputer.

BLOCK 10. SIDETONE OSCILLATOR

U49 is a Schmidt trigger nand gate used as a gated oscillator. When a BELL signal is commanded by the microcomputer, U49 goes into oscillation. The frequency of operation is equivalent to the frequency of the mark tone and allows zero beating of the input signal for tuning purposes in the Morse code receive mode. Q6 and Q7 buffer the output of U49 for presentation to the speaker.

BLOCK 11. SINE WAVE SYNTHESIZER

Shift register U48 is used as digital sine wave synthesizer by summing its outputs in a weighted resistor network. The result is a 16 step sine wave approximation. The input clock is 16 times the desired output frequency and is provided by the U3 timer output. U63 forms a second order lowpass filter for smoothing the discrete voltage steps produced by the sine wave generator.

ACTIVE DEVICE LIST

IC LIST

SYMBOL	TYPE	FUNCTION
U1	8085A	MICROPROCESSOR
U2	8155	RAM, I/O, TIMER
U3	8155	RAM, I/O, TIMER
U4	74LS373	ADDRESS LATCH
U5	2732	READ ONLY MEMORY
U6	2716	READ ONLY MEMORY
U7	8251A	USART
U8	74LS374	BASE ADDRESS REGISTER
U9	74LS163	CHARACTER ADDRESS GENERATOR
U10	74LS374	ROW ADDRESS REGISTER
U11	74LS163	CHARACTER ADDRESS GENERATOR
U12	74LS30	END OF MEMORY DECODER
U13	74LS163	DOT COUNTER
U14	74LS163	CHARACTER COUNTER
U15	74LS163	CHARACTER COUNTER
U16	74LS163	CHARACTER DOT LINE COUNTER
U17	74LS163	CHARACTER ROW COUNTER
U18	74LS163	CHARACTER ROW COUNTER
U19	74LS138	ADDRESS DECODER
U20	74LS243	BUS CONTROLLER
U21	74LS243	BUS CONTROLLER
U22	2316	CHARACTER GENERATOR ROM
U23	74166	VIDEO SHIFT REGISTER
U24	74LS157	ADDRESS MULTIPLEXER
U25	74LS157	ADDRESS MULTIPLEXER
U26	74LS157	ADDRESS MULTIPLEXER
U27	2114	1K X 4 VIDEO DISPLAY RAM
U28	2114	1K X 4 VIDEO DISPLAY RAM
U29	2114	1K X 4 VIDEO DISPLAY RAM
U30	2114	1K X 4 VIDEO DISPLAY RAM
U31	74LS74	CHARACTER LINE-0 DECODER
U32	74LS86	BLANKING GATE, VIDEO INVERT GATE
U34	74LS10	HORIZONTAL AND VERTICAL SYNC DECODER
U35	74LS32	CPU READY/WAIT GATE
U36	74LS02	BLANKING COMBINER, BUS CONTROL GATE
U37	74LS00	HORIZONTAL SYNC FLIP-FLOP, BUS CONTROL GATE
U38	74LS04	CLOCK BUFFER, HORIZONTAL AND VERTICAL TIMING GATE
U39	74LS175	PROCESSOR CLOCK, CLOCK RETIMING
U40	74LS00	VERTICAL SYNC FLIP-FLOP, ADDRESS GENERATOR
U41	7438	VIDEO COMBINER
U42	74LS20	4K ROM ENABLE, ADDRESS GENERATOR GATE
U44	74LS02	HORIZONTAL AND VERTICAL TIMING GATE
U45	7404	SYSTEM CLOCK, HORIZONTAL AND VERTICAL TIMING GATE
U46	74LS30	KEYPRESS DECODER
U47	1458	TUNING INDICATOR
U48	74LS164	SINE WAVE GENERATOR
U49	74LS132	SIDETONE OSCILLATOR, REPEAT KEY OSCILLATOR AND GATE
U50	1458	HIGH-PASS FILTER
U51	TL191	170HZ/850HZ FILTER SELECT
U52	1458	LOW-PASS FILTER
U53	1458	LIMITER
U54	1458	SLICER
U56	1458	LOW-PASS FILTER
U57	1458	FULL WAVE RECTIFIER
U58	TL191	170HZ/850HZ FILTER SELECT

U59	1458	850HZ MARK BANDPASS FILTER
U60	1458	170HZ MARK BANDPASS FILTER
U61	1458	850HZ SPACE BANDPASS FILTER
U62	1458	170HZ SPACE BANDPASS FILTER
U63	1458	LOW PASS FILTER
U64	74LS86	DATA REVERSE/NORMAL GATE, SINE WAVE GENERATOR GATE

TRANSISTOR LIST

SYMBOL	TYPE	FUNCTION
Q1	2N4124	VIDEO OUTPUT
Q2	MJE350	CW KEYER DRIVER
Q3	MJE340	CW KEYER
Q4	TIP48	TTY LOOP KEYER
Q5	MJE340	TRANSMIT/RECEIVE SWITCH
Q6	2N4124	SIDETONE DRIVER
Q7	2N4126	SIDETONE DRIVER

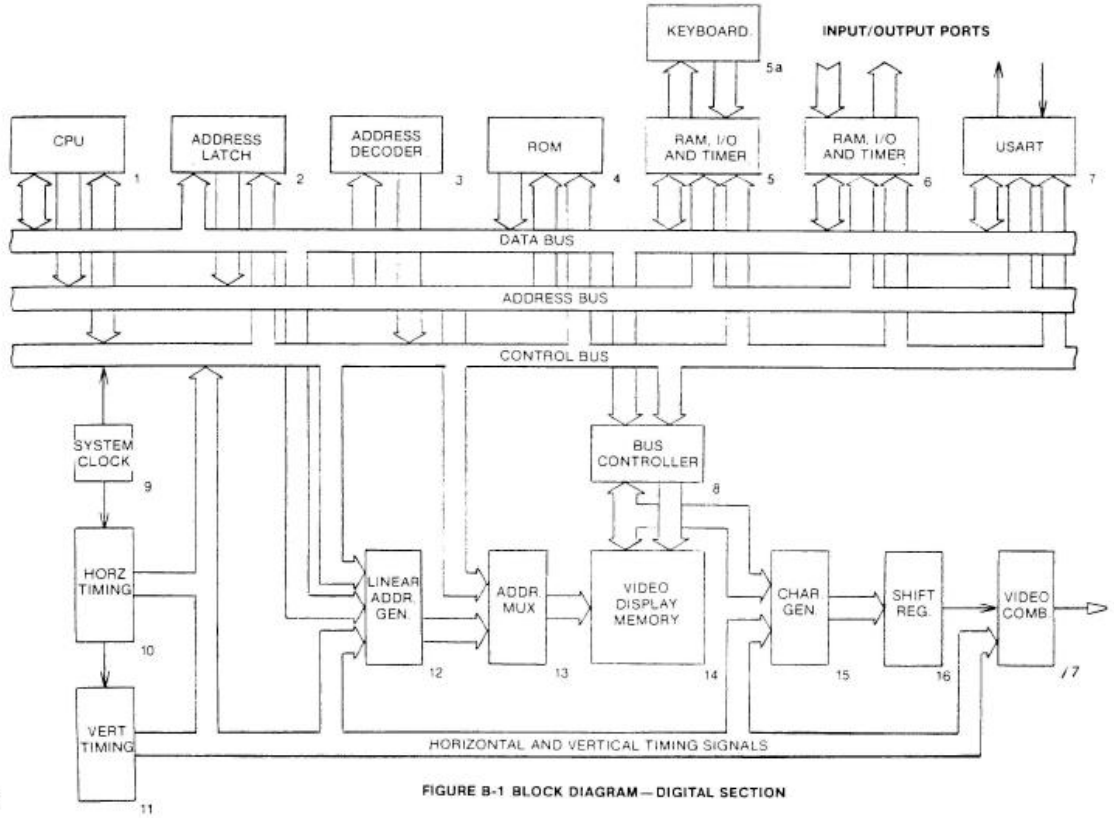

FIGURE B-1 BLOCK DIAGRAM—DIGITAL SECTION

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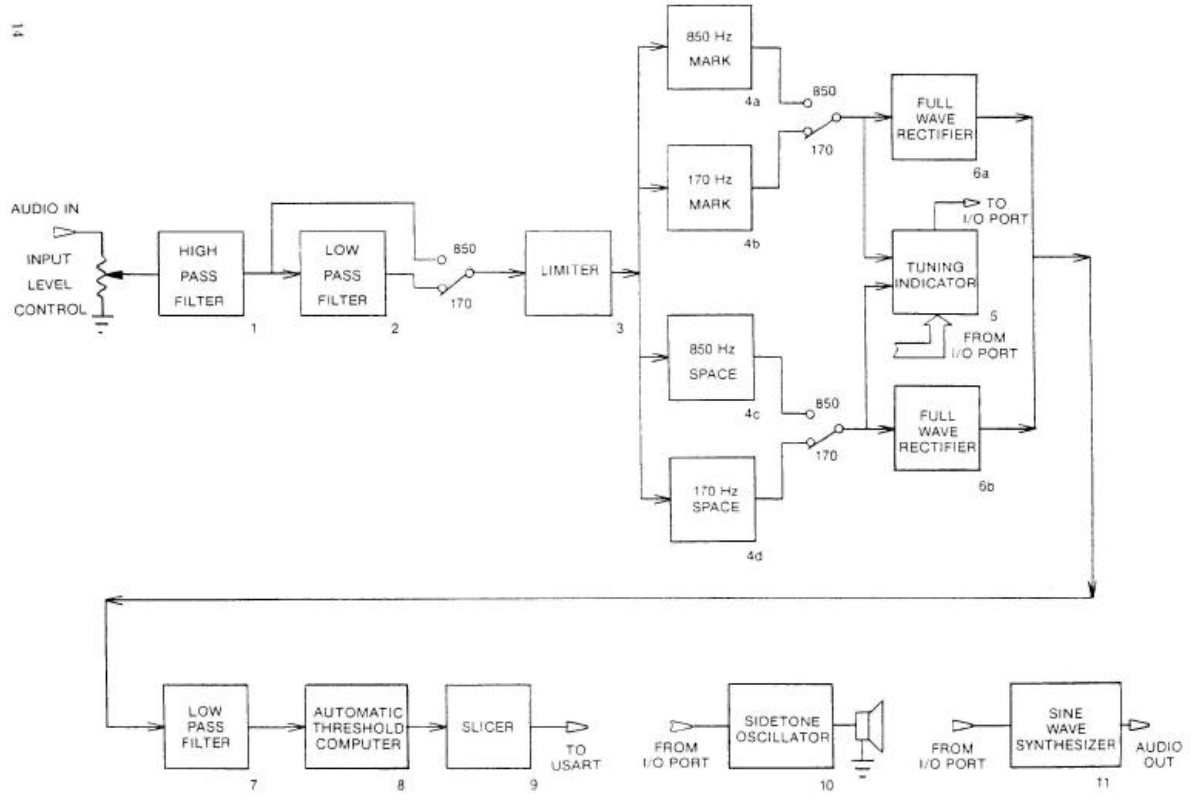

FIGURE B-2 BLOCK DIAGRAM—ANALOG SECTION

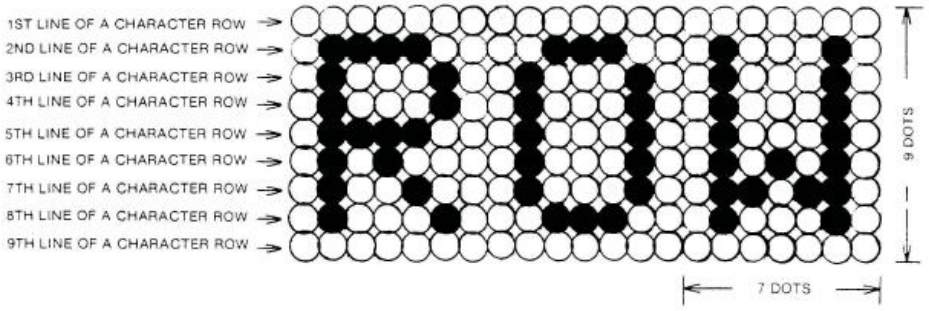

FIGURE 8-3 CHARACTER GENERATION

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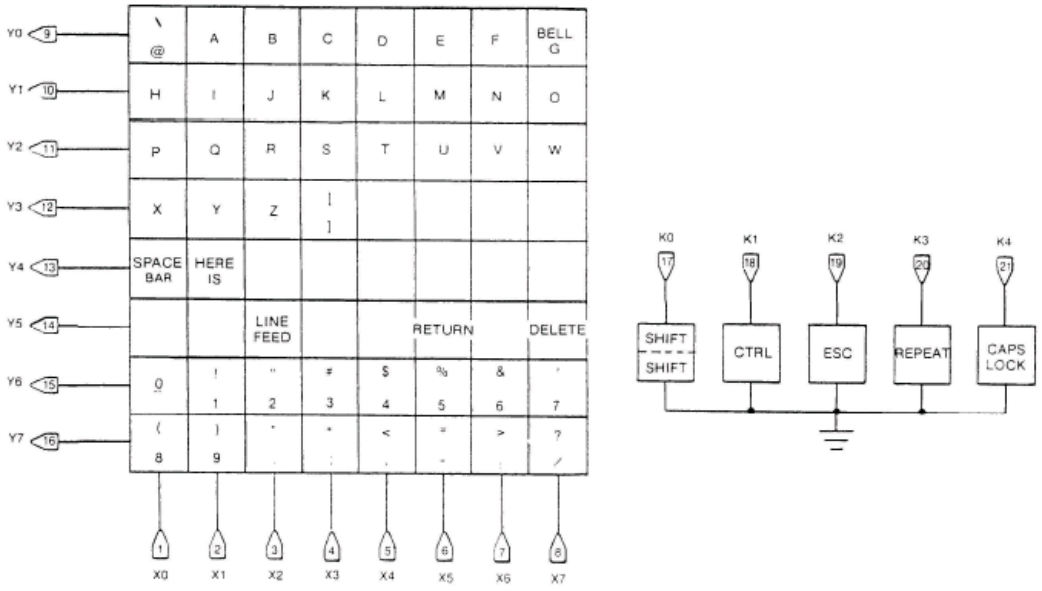

FIGURE C-1 KEYBOARD MATRIX

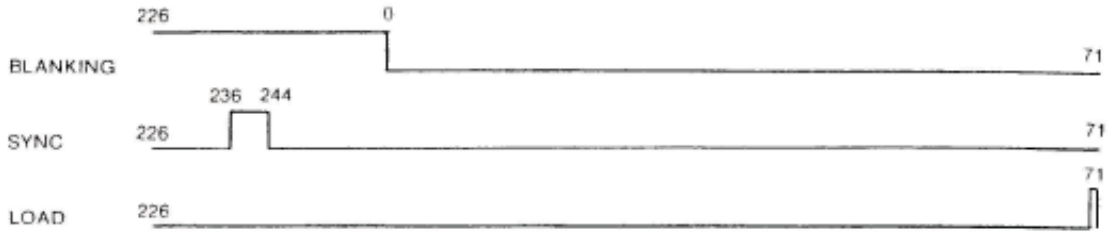

FIGURE C-2 HORIZONTAL TIMING

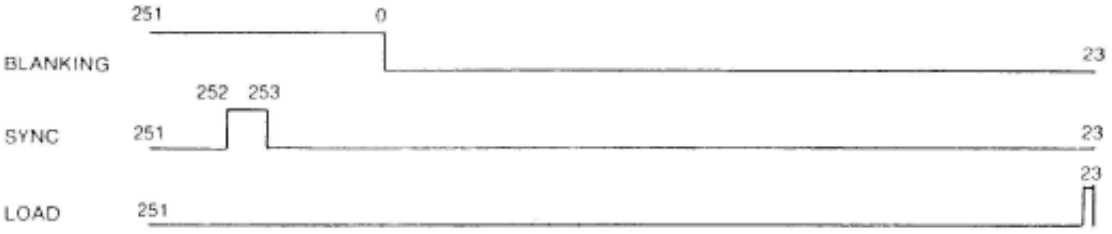

FIGURE C-3 VERTICAL TIMING—60 Hz

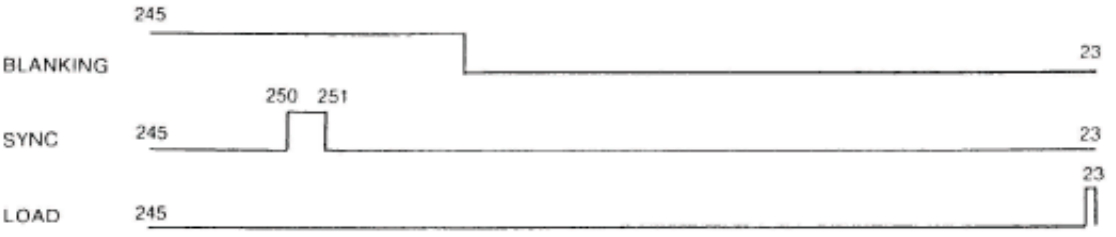

FIGURE C-4 VERTICAL TIMING—50 Hz

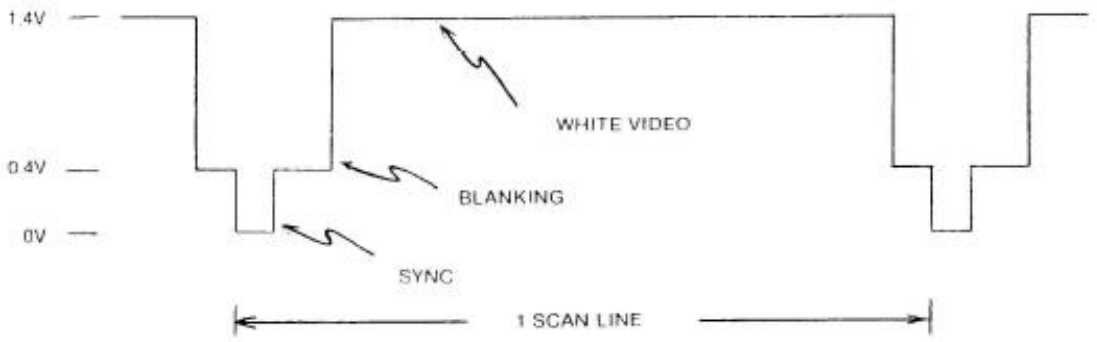

FIGURE C-5 COMPOSITE VIDEO OUTPUT